DECLARATION

I, Tadashi HASHIMOTO , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

1) THAT I am well acquainted with the Japanese language and English language, and

2) THAT the attached is a full, true, accurate and faithful translation into the English language made by me of Japanese Patent Application No. 2001-008301

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 22nd day of December , 2004 .

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[Claims]

[Claim 1]

A semiconductor device, comprising:

a semiconductor substrate;

a gate insulation film formed on one major surface of said semiconductor substrate and containing titanium oxide as a primary constituent material; and

a gate electrode film formed in contact with said gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material.

[Claim 2]

A semiconductor device according to claim 1,

wherein film thickness of said gate insulation film and said gate electrode film is greater than 0.9 nm inclusive.

[Claim 3]

A semiconductor device according to claim 1 or 2,

wherein said titanium oxide is in the form of a crystal of rutile structure.

[Claim 4]

A semiconductor device, comprising:

a semiconductor substrate;

a gate insulation film formed on one major surface of said semiconductor substrate and containing titanium oxide as a primary constituent material; and

a gate electrode film formed in contact with said gate insulation film,

wherein said gate electrode film is constituted by a multilayer film which is composed of an electrically conductive oxide film containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and an electrically conductive film containing a metal as a primary constituent material.

[Claim 5]

A semiconductor device according to claim 4,

wherein film thickness of said gate insulation film and said electrically conductive oxide film is greater than 0.9 nm inclusive.

[Claim 6]

A semiconductor device according to claim 4 or 5,

wherein said titanium oxide is in the form of a crystal of rutile structure.

[Claim 7]

A semiconductor device according to one of Claims 4, 5 and 6,

wherein said metal is ruthenium or alternatively iridium.

[Claim 8]

A semiconductor device, comprising:

a semiconductor substrate;

a gate insulation film formed on one major surface of said semiconductor substrate and containing titanium oxide as a primary constituent material;

a gate electrode film formed in contact with said gate insulation film and constituted by a multilayer film which is composed of an electrically conductive oxide film containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and an electrically conductive film containing a metal as a primary constituent material;

a first capacitor electrode formed on the one major surface of said semiconductor substrate;

a capacitor insulation film formed in contact with said first capacitor electrode and exhibiting a high dielectric constant or alternatively ferroelectricity; and

a second capacitor electrode formed in contact with said capacitor insulation film.

[Claim 9]

A semiconductor device according to claim 8,

wherein film thickness of said insulation film and said electrically conductive oxide film is greater

than 0.9 nm inclusive.

[Claim 10]

A semiconductor device according to claim 8, wherein said titanium oxide is in the form of a crystal of rutile structure.

[Claim 11]

A semiconductor device according to claim 8, wherein said metal is ruthenium or alternatively iridium.

[Claim 12]

A semiconductor device, comprising:

a semiconductor substrate;

a gate insulation film composed of a first gate insulation film formed on one major surface of said semiconductor substrate and containing titanium oxide and titanium silicate as primary constituent materials and a second gate insulation film formed on said one major surface and containing titanium oxide as a primary constituent material; and

a gate electrode film formed in contact with said gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material.

[Claim 13]

A semiconductor device, comprising:

a semiconductor substrate;

a gate insulation film composed of a first

gate insulation film formed on one major surface of said semiconductor substrate and containing titanium oxide and titanium silicate as primary constituent materials and a second gate insulation film formed on said one major surface and containing titanium oxide as a primary constituent material; and

a gate electrode composed of a first gate electrode film formed in contact with said gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and a second gate electrode film formed in contact with said gate insulation film and containing one selected from a group consisting of ruthenium, iridium, platinum, tungsten and molybdenum as a primary constituent material.

[Claim 14]

A method of manufacturing a semiconductor device, comprising the steps of:

forming a gate insulation film containing titanium oxide as a primary constituent material on one major surface of a semiconductor substrate; and

depositing on said gate insulation film a conductor film containing ruthenium or alternatively iridium as a primary constituent material to thereby form a gate electrode film.

[Claim 15]

A method of manufacturing a semiconductor

device, comprising the steps of:

forming a gate insulation film containing titanium oxide as a primary constituent material on one major surface of a semiconductor substrate;

depositing on said gate insulation film a conductor film containing ruthenium or alternatively iridium as a primary constituent material to thereby form a gate electrode film;

forming a first capacitor electrode;

forming a capacitor insulation film having high dielectric constant or ferroelectricity in contact with said silicon first capacitor electrode; and

forming a second capacitor electrode in contact with said capacitor insulation film.

[Detailed Description of the Invention]

[0001]

[Technical Field Pertinent to the Invention]

The present invention relates to a semiconductor device and a method of manufacturing the same.

[0002]

[Prior Art]

In recent years, in keeping with a trend of implementing the semiconductor device in a miniaturized structure, there has arisen the requirement that the gate of a transistor be realized in a length of 0.15 μm

with the film thickness of the gate insulation film being decreased to less than 2 nm when silicon oxide (SiO_2) is employed for the gate insulation film.

[0003]

In this conjunction, it is noted that such thickness of the gate insulation film as mentioned above will give rise to occurrence of a tunnel current of unignorable magnitude.

[0004]

To cope with this problem, it has been attempted to increase the physical film thickness while maintaining the desired dielectric characteristic by using an insulation material exhibiting higher dielectric constant than SiO_2.

As a candidate for such high dielectric constant material, there may be mentioned titanium oxide, as is reported in the collection of lecture reprints of "THE 1999 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS", pp. 164-165.

[0005]

[Problem to be solved by the Invention]

However, in the present state of the art, when the semiconductor device is formed by using titanium oxide for the gate insulation film in actuality, a leak current will flow through the gate insulation film of titanium oxide, degrading the reliability of the semiconductor device.

[0006]

Such being the circumstances, there exists a demand for practical implementation of the semiconductor device in which the occurrence of the leak current is suppressed by increasing the physical film thickness while maintaining the dielectric characteristic.

[0007]

An object of the present invention is to provide a semiconductor device in which the occurrence of leak current is suppressed by increasing the physical film thickness while maintaining the dielectric characteristic and also provide a method of manufacturing the same.

[0008]

[Means for Solving the Problem]

The inventors of the present application have made studies for making clear the causes for occurrence of leak current in the semiconductor devices and found that one of the major causes for the leak current resides in that silicon elements of the gate electrode formed of e.g. polycrystalline silicon diffuse into the titanium oxide film upon heat treatment in the course of manufacturing process.

[0009]

Further, it has been discovered that the diffusion mentioned above is more likely to take place as the temperature for heat treatment is higher and

makes appearance more remarkably in memory products in which a capacitor insulation film exhibiting a high dielectric constant or ferroelectricity and which undergo heat treatment at higher temperature although the diffusion phenomenon is certainly observed in the logic LSI devices as well.

[0010]

Furthermore, as a result of strenuous studies for finding out the means for preventing diffusion of conductive elements into the gate insulation film formed of titanium oxide from the gate electrode, the inventors of the present application have discovered that use of ruthenium oxide or iridium oxide as the gate electrode material to be formed in contact with titanium oxide is effective for suppressing the occurrence of current leakage mentioned above.

[0011]

At this juncture, it should be mentioned that silicon element and metal elements are herein also referred to as conductive element(s) only for the convenience of description.

[0012]

For achieving the object mentioned previously, the teachings of the present invention are incarnated in the embodiments enumerated below.

(1) A semiconductor device includes a semiconductor substrate, a gate insulation film formed

on one major surface of the semiconductor substrate and containing titanium oxide as a primary constituent material, and a gate electrode film formed in contact with the gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material.

[0013]

(2) In the semiconductor device set forth in the above paragraph (1), film thickness of the gate insulation film and the conductive oxide film is preferably greater than 0.9 nm inclusive.

[0014]

(3) In the semiconductor device set forth in the above paragraph (1) or (2), titanium oxide is preferably in the form of a crystal of rutile structure.

[0015]

(4) A semiconductor device includes a semiconductor substrate, a gate insulation film formed on one major surface of the semiconductor substrate and containing titanium oxide as a primary constituent material, and a gate electrode film formed in contact with the gate insulation film, wherein the gate electrode film is constituted by a multilayer film which is composed of an electrically conductive oxide film containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and an electrically conductive film containing a metal as a

primary constituent material.

[0016]

(5) Further, in the semiconductor device set forth in the above paragraph (4), film thickness of the gate insulation film and the electrically conductive oxide film are preferably greater than 0.9 nm inclusive.

[0017]

(6) In the semiconductor device set forth in the above paragraph (4) or (5), titanium oxide is preferably in the form of a crystal of rutile structure.

[0018]

(7) Furthermore, in the semiconductor device set forth in the above paragraph (4), (5) or (6), the metal is preferably ruthenium or alternatively iridium.

[0019]

(8) A semiconductor device includes a semiconductor substrate, a gate insulation film formed on one major surface of the semiconductor substrate and containing titanium oxide as a primary constituent material, a gate electrode film formed in contact with the gate insulation film and constituted by a multilayer film which is composed of an electrically conductive oxide film containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and an electrically conductive film containing a metal as a primary constituent material, a first capacitor electrode formed on the one major surface of the semi-

conductor substrate, a capacitor insulation film formed in contact with the first capacitor electrode and exhibiting a high dielectric constant or alternatively ferroelectricity, and a second capacitor electrode formed in contact with the capacitor insulation film.

[0020]

(9) Further, in the semiconductor device set forth in the above paragraph (8), film thickness of the insulation film and the electrically conductive oxide film are preferably greater than 0.9 nm inclusive.

[0021]

(10) In the semiconductor device set forth in the above paragraph (8), titanium oxide is preferably in the form of a crystal of rutile structure.

[0022]

(11) Furthermore, in the semiconductor device set forth in the above paragraph (8), the metal is preferably ruthenium or alternatively iridium.

[0023]

(12) A semiconductor device includes a semiconductor substrate, a gate insulation film composed of a first gate insulation film formed on one major surface of the semi-conductor substrate and containing titanium oxide and titanium silicate as primary constituent materials and a second gate insulation film formed on the one major surface and containing titanium oxide as a primary constituent material, and a gate

electrode film formed in contact with the gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material.

[0024]

(13) A semiconductor device includes a semiconductor substrate, a gate insulation film composed of a first gate insulation film formed on one major surface of the semiconductor substrate and containing titanium oxide and titanium silicate as primary constituent materials and a second gate insulation film formed on the one major surface and containing titanium oxide as a primary constituent material, and a gate electrode composed of a first gate electrode film formed in contact with the gate insulation film and containing ruthenium oxide or alternatively iridium oxide as a primary constituent material and a second gate electrode film formed in contact with the gate insulation film and containing one selected from a group consisting of ruthenium, iridium, platinum, tungsten and molybdenum as a primary constituent material.

[0025]

(14) A method of manufacturing a semiconductor device includes the steps of forming a gate insulation film containing titanium oxide as a primary constituent material on one major surface of a semiconductor substrate, and depositing on the gate insulation film a

conductor film containing ruthenium or alternatively iridium as a primary constituent material to thereby form a gate electrode film.

[0026]

(15) A method of manufacturing a semiconductor device includes the steps of forming a gate insulation film containing titanium oxide as a primary constituent material on one major surface of a semiconductor substrate, depositing on the gate insulation film a conductor film containing ruthenium or alternatively iridium as a primary constituent material to thereby form a gate electrode film, forming a first capacitor electrode, forming a capacitor insulation film having high dielectric constant or ferroelectricity in contact with the silicon first capacitor electrode, and forming a second capacitor electrode in contact with the capacitor insulation film.

[0027]

[Mode for Carrying Out the Invention]

In the following, typical embodiments of the present invention will be described in detail by reference to the drawings. Figure 1 is a sectional view showing schematically a structure of a major portion in the semiconductor device according to a first embodiment of the present invention.

[0028]

In the semiconductor device in the first

embodiment of the present invention, MOS transistors are made by forming diffusion layers 2, 3, 4 and 5 on a silicon substrate 1, and additionally forming gate insulation films 6 and 7 and gate electrodes 8 and 9 on those diffusion layers.

[0029]

To meet the requirements for microminiaturization and higher function, the gate insulation films 6 and 7 are formed by titanium oxide as the primary constituent material. The gate insulation films 6 and 7 are deposited by chemical vapor deposition, sputtering, for example.

[0030]

As the primary constituent material of the gate electrodes 8 and 9, ruthenium oxide or iridium oxide is used because those oxides are materials from which conductive elements are less liable diffuse into the gate insulation films 6, 7 during heat treatment.

[0031]

The "primary constituent material" is defined as a material which occupies 50% or more of the composition of the material of each part.

[0032]

These gate electrodes 8 and 9 may be formed by resorting to, for example, a chemical vapor deposition process, a sputtering process or the like. The MOS transistors are separated from one another by using, for

example, an element separation film 10 constituted by a silicon oxide film.

[0033]

Further, insulation films 11 and 12 each constituted by e.g. a silicon oxide film are formed on top surfaces and side wall surfaces of the gate electrodes 8 and 9, respectively. Formed over the whole top surface of the MOS transistor is an insulation film 13 which may be constituted by e.g. a BPSG (Boron-Doped Phosphor Silicate Glass) film, an SOG (Spin-On-Glass) film or alternatively a silicon oxide film or a nitride film formed through the chemical vapor deposition process or sputtering process.

[0034]

Formed in each of contact holes pierced through the insulation film 13 is a plug composed of a main conductor film 15 which is coated with adjacent conductor films (first conductor films) 14a and 14b for the purpose of preventing the diffusion, wherein the plugs are connected to the diffusion layers 2, 3, 4 and 5, respectively.

[0035]

Through the medium of the plug constituted by the main conductor film 15, first laminated wiring conductors each composed of a main conductor film 17 coated with adjacent conductor films 16a and 16b for preventing the diffusion are connected to the diffusion

layers 2, 3, 4 and 5. The first laminated wiring conductor can be implemented by forming a wiring pattern by etching the adjacent conductor film 16b formed through a sputtering process or the like on the main conductor film 17 also formed by a sputtering process or the like after depositing the adjacent conductor film 16a by a sputtering process. The respective main conductor films 17 are separated electrically by insulating films 18.

[0036]

Formed on the first multilayer wiring conductor is a plug composed of a main conductor film 20 coated with an adjacent conductor film 19 in the contact hole formed in an insulation film 21, which plug is connected to the first laminated wiring conductor.

[0037]

Through the medium of the plug constituted by the main conductor film 20, a second multilayer wiring conductor constituted by a main conductor film 23 coated with adjacent conductor films 22a and 22b is connected to the first laminated wiring conductor.

[0038]

The second laminated wiring conductor constituted by the main conductor film 23 may be implemented by forming a wiring pattern by etching the adjacent conductor film 22b formed by a sputtering process or the like on the main conductor film 23 also

formed by a sputtering process after depositing the adjacent conductor film 22a by s sputtering process. After wirings are formed, insulating films 24 and 25 are formed.

[0039]

In the first embodiment of the present invention, ruthenium oxide or iridium oxide is employed as a primary constituent material for forming the gate electrodes 8 and 9 because with the gate electrodes of ruthenium oxide and iridium oxide, the conductive elements are less liable to diffuse into titanium oxide. By virtue of this feature, leak current can be prevented which will otherwise take place due to the diffusion of elements into the gate insulation films 6 and 7 during heat treatment.

[0040]

In conjunction with the diffusion of elements into titanium oxide, the advantageous effects attained with the semiconductor device according to the first embodiment of the present invention will be described below by comparing ruthenium oxide or iridium oxide employed in the first embodiment of the invention with polycrystalline silicon, tungsten, tungsten silicide, molybdenum, molybdenum silicide, titanium and titanium nitride which have heretofore been examined as the gate insulation film material.

[0041]

For elucidating the effects obtained with the first embodiment of the present invention, analysis examples based on the molecular dynamics simulation are given below.

[0042]

Molecular dynamics simulation is a method for calculating forces acting on individual atoms on the basis of interatomic potentials, and solving Newton's equation of motion for these forces to thereby calculate the positions of the atoms at discrete time points, as is described, for example, in "JOURNAL OF APPLIED PHYSICS", Vol. 54, pp. 4864-4878 (1983).

[0043]

Incidentally, in the first embodiment of the present invention, relations described below could be determined by calculating the interactions among disparate elements by taking into consideration the charge transfer in the molecular dynamics method.

[0044]

A major effect obtained with the first embodiment of the present invention can be seen in that the diffusion of elements into the gate insulation film from the gate electrode can be suppressed.

[0045]

Accordingly, by calculating the diffusion coefficients of conductive elements diffusing into the gate insulation film and comparing the diffusion

coefficients, the effect obtained with the first embodiment of the present invention can analytically be determined.

[0046]

The method of calculating the diffusion coefficient through the molecular dynamics simulation is described, for example, in "PHYSICAL REVIEW B", Vol. 29, pp. 5363 to 5371 (1984).

[0047]

In the first place, the effects obtained with the first embodiment of the present invention will be described in conjunction with calculation examples of the diffusion coefficients in the device of a stacked structure of the gate electrode film of 3 nm in film thickness and the gate insulation film of 3 nm in film thickness.

[0048]

As the gate insulation film, a titanium oxide film of rutile structure or anatase structure was used while as the gate electrode material, there were employed polycrystalline silicon, tungsten, tungsten silicide, molybdenum, molybdenum silicide, titanium and titanium nitride which have heretofore been examined as the gate insulation film material and ruthenium oxide and iridium oxide used in the first embodiment of the present invention.

[0049]

Figure 2 is a graph illustrating the results of calculation of the diffusion coefficients of elements of the gate electrode diffusing into the titanium oxide film of rutile structure at 300°C. Further, Fig. 3 is a view for graphically illustrating the results of calculation of the diffusion coefficients at 600°C.

[0050]

From Figs. 2 and 3, it can be seen that when compare with the other materials, the diffusion coefficient is small in the case where ruthenium oxide or iridium oxide is employed for forming the gate electrode either at 300°C or 600°C.

[0051]

Namely, it can be said that in the case where ruthenium oxide or iridium oxide is used as the gate electrode, elements of the gate electrode are difficult to enter or diffuse into the gate insulation film, ensuring thus enhanced reliability.

[0052]

Shown in Figs. 2 and 3 are the results of calculation for the exemplary case where titanium oxide of the rutile structure is used. On the other hand, the results of calculation of the diffusion coefficients for the exemplary case where titanium oxide of anatase structure is used are shown in Figs. 4 and 5.

[0053]

More specifically, Figs. 4 and 5 are graphs

illustrating the results of calculation of the diffusion coefficients at 300°C and 600°C, respectively. It can also be seen from Figs. 4 and 5 that also when titanium oxide of anatase structure is used, the gate electrode of ruthenium oxide or iridium oxide exhibits smaller diffusion coefficient when compared with the other materials, just like in the examples shown in Figs. 2 and 3.

[0054]

Comparison of the results of calculation illustrated in Figs. 2 and 3 with the results of calculation illustrated in Figs. 4 and 5 shows that smaller diffusion coefficient can be obtained in the case where titanium oxide of rutile structure is employed when compared with the case where titanium oxide of anatase structure is employed.

[0055]

Accordingly, it is preferred to employ titanium oxide of rutile structure for the gate insulation film while ruthenium oxide or iridium oxide is employed for the gate electrode.

[0056]

The gate insulation film of titanium oxide of rutile structure may be deposited at a high temperature, or firstly deposited at a low temperature and subsequently subjected to heat treatment, as is described, for example, in "IBM JOURNAL OF RESEARCH AND

DEVELOPMENT", Vol. 43, No. 3 (May, 1999), pp.383 to 391.

[0057]

The examples shown in Figs. 2, 3, 4 and 5 represent the results of calculation performed when the film thickness of the gate insulation film and the gate electrode film, respectively, is 3 nm. To examine the dependence of the diffusion coefficient on the film thickness, further examination was conducted and, the examination results with the film thickness varied will be described below.

[0058]

Figures 6 and 7 are graphs showing results of calculations made when the film thickness of both the gate insulation film and the gate electrode film is 0.9 nm each and the temperature is 300°C. Fig. 6 shows the case where the gate insulation film is formed of titanium oxide of rutile structure while Fig. 7 shows the case where the gate insulation film is formed of titanium oxide of anatase structure.

[0059]

As can be seen from Figs. 6 and 7, even when the film thickness is thinned down to 0.9 nm, the diffusion coefficients with ruthenium oxide and iridium oxide are significantly small when compared with the others, as in the case where the film thickness is 3 nm.

[0060]

Furthermore, also when the temperature is

600°C, the results of calculation shows that the diffusion coefficients for ruthenium oxide and iridium oxide are significantly small when compared with the others, although not shown in the drawing.

[0061]

By contrast, Fig. 8 graphically shows the results of calculation for the rutile structure at 300°C in the case where the thickness of the gate electrode film is 0.8 nm with the film thickness of the gate insulation film unchanged at 0.9 nm.

[0062]

In the case of the example shown in Fig. 8, diffusion coefficients of ruthenium oxide and iridium oxide increase remarkably as compared with the examples shown in Figs. 6 and 7, indicating that the effect in the first embodiment of the present invention is reduced slightly.

[0063]

Accordingly, the film thickness of ruthenium oxide or iridium oxide should preferably be greater than 0.9 nm inclusive.

[0064]

Next, Fig. 9 graphically shows the results of calculation for the rutile structure at 300°C in the case where the thickness of the gate insulation film is 0.8 nm with the film thickness of the gate electrode film unchanged at 0.9 nm. Also in the case of the example

shown in Fig. 9, diffusion coefficients of ruthenium oxide and iridium oxide increase remarkably when compared with the examples shown in Figs. 6 and 7, indicating that the effect in the first embodiment of the present invention reduced slightly.

[0065]

Therefore, the film thickness of titanium oxide should also preferably be greater than 0.9 nm inclusive. The examples shown in Figs. 8 and 9 are with the rutile structure, but the results suggest that for the titanium oxide film of the anatase structure, too, the film thickness should preferably be greater than 0.9 nm inclusive. The reason why the effect is lessened with the film thickness of less than 0.8 nm is because the crystal structure of ruthenium oxide, iridium oxide and titanium oxide becomes slightly unstable.

[0066]

As is apparent from the foregoing, the first embodiment, a semiconductor device can be realized in which occurrence of the leak current can positively be suppressed by increasing the physical film thickness while ensuring the dielectric characteristic by virtue of the feature that the gate electrodes 8 and 9 are implemented by using as the primary constituent material ruthenium oxide and iridium oxide with which diffusion into titanium oxide is difficult to occur.

[0067]

Next, a semiconductor device according to a second embodiment of the present invention will be described. Fig. 10 shows a sectional structure of a major portion of the semiconductor device according to the second embodiment of the invention.

[0068]

The main difference of the second embodiment from the first embodiment is that the respective gate insulation films are formed in a two-layer structure, including a first gate insulation film 6a, 7a and a second gate insulation film 6b, 7b.

[0069]

To meet the requirements for miniaturization and high performance, titanium oxide is used as a primary constituent material to form the second gate insulation films 6b, 7b. Silicon oxide or titanium silicate, for example, is used as a primary constituent material to form the first gate insulation films 6a, 7a. Thus, a resulting effect is that the second gate insulation films 6b, 7b has been improved in thermal stability.

[0070]

Thus, with the second embodiment of the present invention, the effect that the thermal stability of the second gate insulation films 6b and 7b is enhanced can be obtained in addition to the effects similar to those mentioned previously in conjunction

with the first embodiment of the invention.

[0071]

At this juncture, the gate insulation film may be implemented in a structure having three or more layers, although illustration thereof is omitted. Fig. 11 which shows a sectional structure of a major portion of the semiconductor device according to the third embodiment of the invention.

[0072]

The main difference of the semiconductor device according to the third embodiment of the invention from the second embodiment is that in the third embodiment, the respective gate electrode films of the semiconductor device are implemented in a two-layer structure including a first gate electrode film 8a; 9a and a second gate electrode film 8b; 9b.

[0073]

As the primary constituent material of the first gate electrode films 8a and 9a, ruthenium oxide or iridium oxide is used with which conductive elements are difficult to diffuse into the second gate insulation film 6b; 7b upon heat treatment.

[0074]

For the second gate electrode film 8b; 9b, a film containing as the primary constituent material one selected from a group consisting of e.g. ruthenium, iridium, platinum, tungsten and molybdenum is employed.

Owing to this feature, an effect can be obtained that the electric resistance of the whole gate electrode is decreased.

[0075]

Thus, with the third embodiment of the present invention, an effect can be obtained that the electric resistance of the gate electrode as a whole is decreased in addition to the effects similar to those mentioned previously in conjunction with the first embodiment of the invention.

[0076]

Figure 12 is a view showing a sectional structure of a memory cell in the semiconductor device according to a fourth embodiment of the present invention. The main difference of the fourth embodiment from the first, second and third embodiments is that in the fourth embodiment, the semiconductor device includes an information storing capacitor element 103 implemented in a stacked structure including a conductive barrier film 114, a capacitor bottom electrode 115, an oxide film 116 exhibiting a high dielectric constant or ferroelectricity and a capacitor top electrode 117.

[0077]

As is generally known, the oxide film 116 having a high dielectric constant or ferroelectricity can not exhibit desired favorable characteristics unless it is heat treated. Thus, heat treatment at about 600°C

or higher and more preferably at about 700°C or higher is required in the manufacturing process.

[0078]

During the heat treatment mentioned above, elements are likely to diffuse into the gate insulation film from the gate electrode film. Accordingly, when a semiconductor memory in which an oxide film having a high dielectric constant or ferroelectricity is used, it becomes all the more necessary to suppress the diffusion described above.

[0079]

A major structure of the semiconductor device according to the fourth embodiment of the invention will be described below. As is shown in Fig. 12, the semiconductor device according to the fourth embodiment of the invention includes a MOS (Metal Oxide Semiconductor) transistor 102 formed in an active region of a major surface of a silicon substrate 101 and an information storing capacitor element 103 disposed on the MOS (Metal Oxide Semiconductor) transistor 102.

[0080]

An insulation film 112 serves as a film for inter-element separation. The MOS transistor 102 of the memory cell is composed of a gate electrode film 105, a gate insulation film 106 and diffusion films 107 and 108. Reference numeral 104 denotes an element separation film. With a view to satisfying the

requirement for miniaturization and better function, titanium oxide is employed as a primary constituent material for forming the gate insulation film 106.

[0081]

The gate insulation film 106 mentioned above is formed by, for example, a chemical vapor deposition process, a sputtering process or the like. Incidentally, the gate insulation film 106 may be implemented in a multi-layer structure having, for example, two or more layers, as in the second and third embodiments of the invention described hereinbefore.

[0082]

As the primary constituent material for the gate electrode film 105, ruthenium oxide or iridium oxide is used because, when the gate electrode is formed by one of those materials, the diffusion of conductive elements into the gate insulation film 106 is difficult to occur in heat treatment. This gate electrode film 105 may be implemented in a multi-layer structure having two or more layers as describe previously in conjunction with the third embodiment of the invention.

[0083]

The gate electrode film 105 is formed by, for example, a chemical vapor deposition process, a sputtering process or the like. Further, an insulation film 109 of silicon oxide film, for example, is formed on the top surface and the side walls of the gate

electrode film 105.

[0084]

A bit line 111 is connected through a plug 110 to one diffusion layer 107 of the MOS transistor for selecting a memory cell. A BPSG (Boron-doped Phospho Silicate Glass) film or an SOG (Spin On Glass) film, or a silicon oxide film or nitride film, which is formed by chemical vapor deposition or sputtering, is deposited on the whole top surface of the MOS transistor.

[0085]

The information-storing capacitor element 103 is formed on the insulation film 112 covering the MOS transistor. The information-storing capacitor element 103 is connected to the other diffusion layer 108 of the memory-cell-selecting MOS transistor through the plug 113 made of polycrystalline silicon.

[0086]

The information-storing capacitor element 103 is formed in a multilayer structure including a conductive barrier film 114, a capacitor bottom electrode 115, an oxide film 116 with high dielectric constant or ferroelectricity and a capacitor top electrode 117 in this order as viewed from the bottom layer. The information-storing capacitor element 103 is covered with an insulation film 118.

[0087]

Also in the fourth embodiment, effects can be

obtained which are similar to those mentioned hereinbefore in conjunction with the first embodiment.

According to a fifth embodiment of the present invention, a system LSI is provided, which has mounted on the same substrate a memory LSI according to the afore-mentioned fourth embodiment and a logic LSI according to the first, second and third embodiments.

[0088]

Also in the fifth embodiment, effects similar to those in the first to the third embodiments can be obtained.

[0089]

As an embodiment of the method for manufacturing a semiconductor of the present invention, there is a method described below.

More specifically, in a first process of the method for manufacturing a semiconductor device according to an embodiment, a gate insulation film made of titanium oxide as a primary constituent material is formed on one major surface of a semiconductor substrate.

[0090]

Then, in a second process, gate electrode films are formed by depositing a conductive film of ruthenium or iridium as a primary constituent material on the gate insulating film.

[0091]

According to the one embodiment described above, it is possible to realize a method for manufacturing a semiconductor device, in which the leak current is prevented by increasing physical film thickness while maintaining the dielectric characteristic.

[0092]

Among other methods for manufacturing a semiconductor device of the present invention, there is another method as described below.

[0093]

More specifically, in a third process of manufacturing a semiconductor according to this other method, a gate insulation film of titanium oxide as a primary constituent material is formed on one primary surface of a semiconductor substrate.

[0094]

The, in a second process, gate electrode films are formed by depositing a conductive film of ruthenium or iridium as a primary constituent material on the gate insulation film.

[0095]

Subsequently, in a third step, a first capacitor electrode is formed and in a fourth step, a capacitor insulation film having a high dielectric constant or ferroelectricity is formed in contact with the first capacitor electrode mentioned above. Finally,

in a fifth step, a second capacitor electrode is formed in contact with the capacitor insulation film mentioned above.

[0096]

According to the manufacturing method described just above, as in the above-mentioned one embodiment, a semiconductor device can be realized in which leak current is prevented by increasing the physical film thickness while maintaining the dielectric characteristic.

[0097]

[Advantages of the Invention]

The present invention provides semiconductor devices in which occurrence of the leak current is prevented by increasing the physical film thickness while maintaining the dielectric characteristic, and also provides methods of manufacturing the same.

[0098]

Further, there are provided a semiconductor device and a method of manufacturing the same which can enjoy high yield and enhanced manufacturing efficiency.

[0099]

Moreover, there are provided a semiconductor device having a gate structure unlikely to incur current leakage and a method of manufacturing the same.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a sectional view showing schematically a structure of a major portion of a semiconductor device according to a first embodiment of the present invention;

[Fig. 2]

Fig. 2 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 3 nm in thickness diffusing into a titanium oxide film of rutile structure of 3 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 3]

Fig. 3 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 3 nm in thickness diffusing into a titanium oxide film of rutile structure of 3 nm in thickness at 600°C in the device according to the first embodiment of the invention;

[Fig. 4]

Fig. 4 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 3 nm in thickness diffusing into a titanium oxide film of anatase structure of 3 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 5]

Fig. 5 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 3 nm in thickness diffusing into a titanium oxide film of anatase structure of 3 nm in thickness at 600°C in the device according to the first embodiment of the invention;

[Fig. 6]

Fig. 6 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 0.9 nm in thickness diffusing into a titanium oxide film of rutile structure of 0.9 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 7]

Fig. 7 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 0.9 nm in thickness diffusing into a titanium oxide film of anatase structure of 0.9 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 8]

Fig. 8 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 0.8 nm in thickness diffusing into a titanium oxide film of rutile structure of 0.9 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 9]

Fig. 9 is a graph illustrating diffusion coefficients of constituent elements of a gate electrode of 0.9 nm in thickness diffusing into a titanium oxide film of rutile structure of 0.8 nm in thickness at 300°C in the device according to the first embodiment of the invention;

[Fig. 10]

Fig. 10 is a sectional view showing generally and schematically a structure of a major portion of a semiconductor device according to a second embodiment of the present invention;

[Fig. 11]

Fig. 11 is a sectional view showing generally and schematically a structure of a major portion of a semiconductor device according to a third embodiment of the present invention; and

[Fig. 12]

Fig. 12 is a sectional view showing generally and schematically a structure of a major portion of a semiconductor device according to a fourth embodiment of the present invention.

[Description of Reference Numerals]

1 Silicon substrate

2, 3, 4, 5 Diffusion layers

6, 6a, 6b Gate electrode films

7, 7a, 7b Gate electrode films

8, 8a, 8b Gate electrodes

9, 9a, 9b Gate electrodes

10 Isolation film

11, 12, 13 Insulation films

18, 21 Insulation films

24, 25 Insulation films

14a, 14b Adjacent conductive films

16a, 16b Adjacent conductive films

19, 22a, 22b Adjacent conductive films

15, 17, 20, 23 Primary conductive films

101 Silicon substrate

102 Transistor

103 Capacitor element for storing information

104 Isolation film

105 Gate electrode film

106 Gate electrode film

107, 108 Diffusion layers

109 Insulation film

110 Plug

111 bit line

112 Insulation film

113 Plugs

114 Barrier film

115 Capacitor bottom electrode

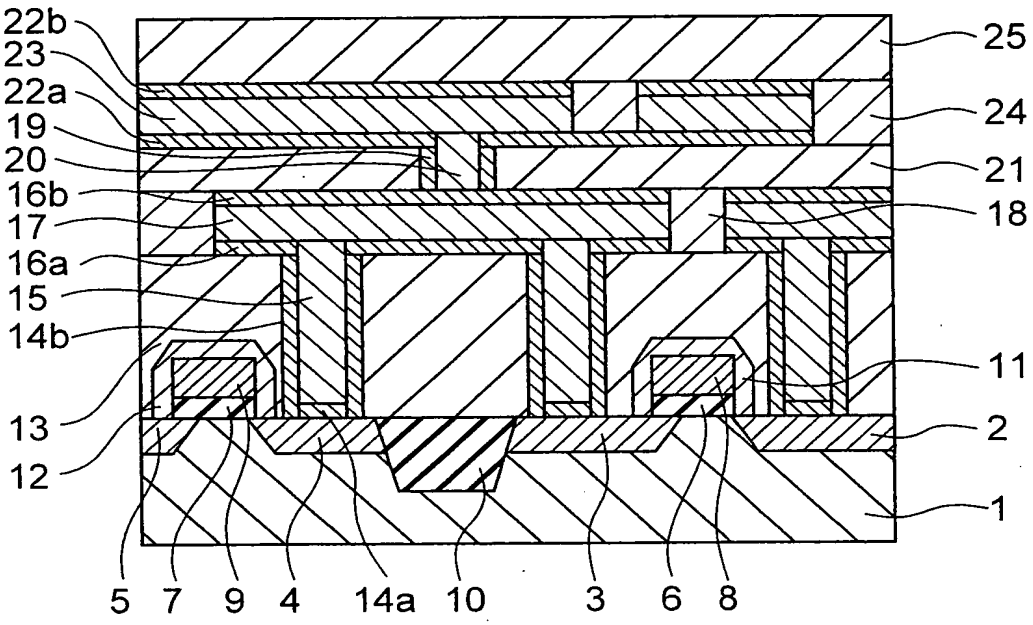
116 Oxide film

117 Capacitor top electrode

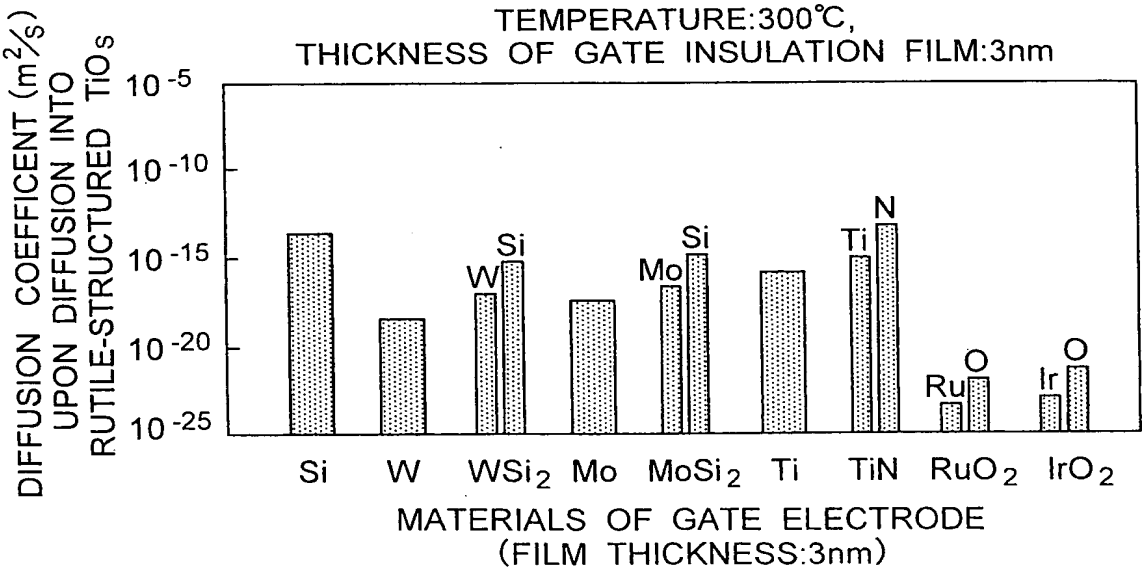
118 Insulation film

[Kind of Document] Drawings

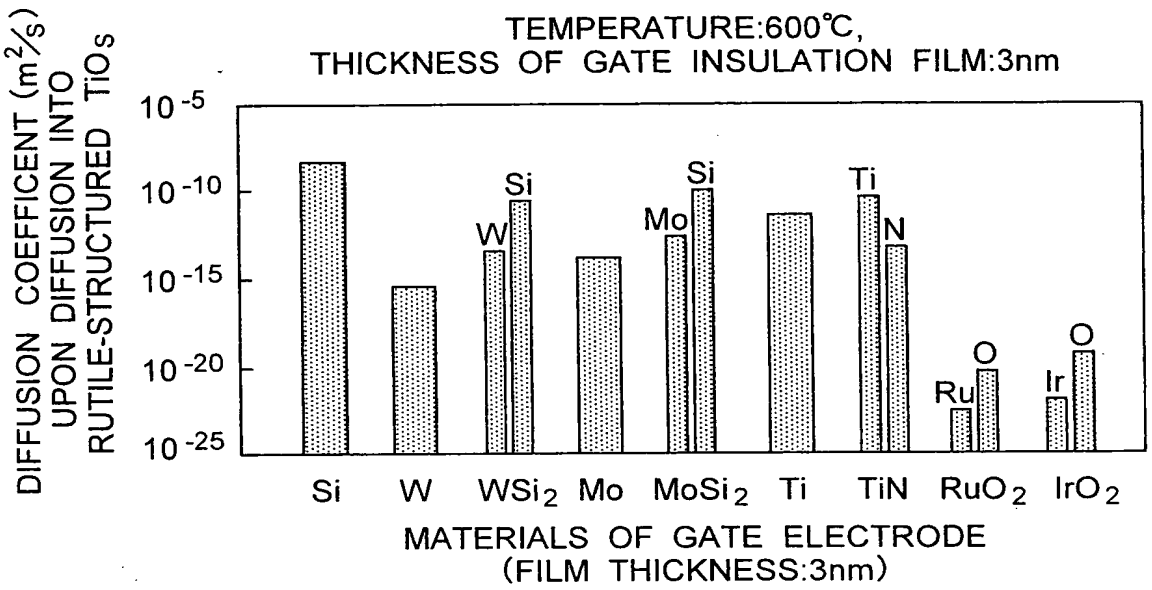
[FIG. 1]



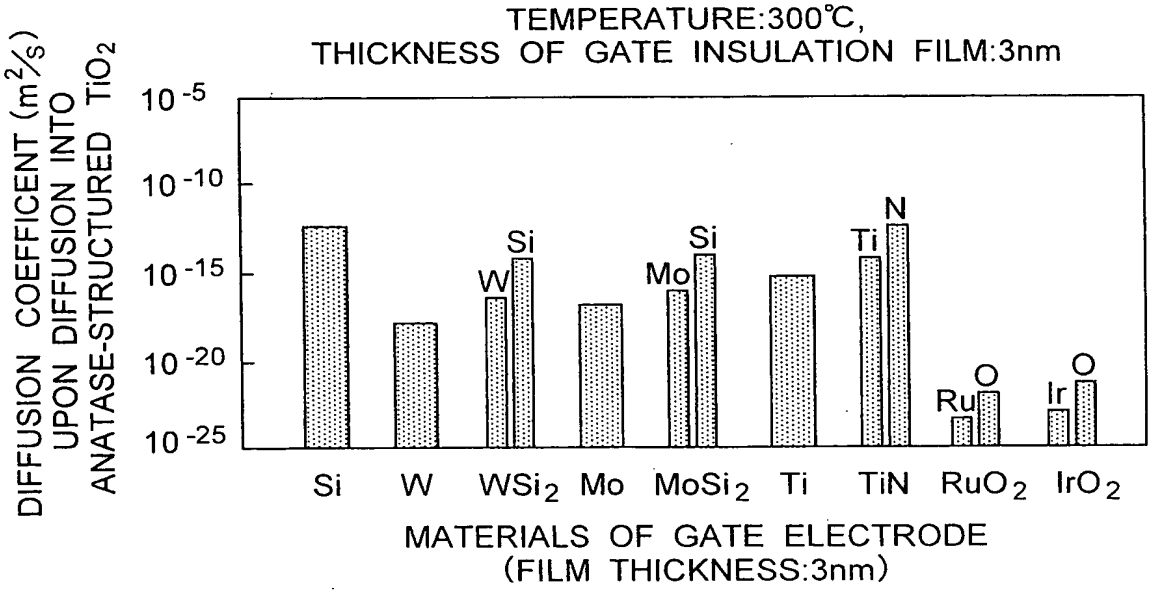
[FIG. 2]



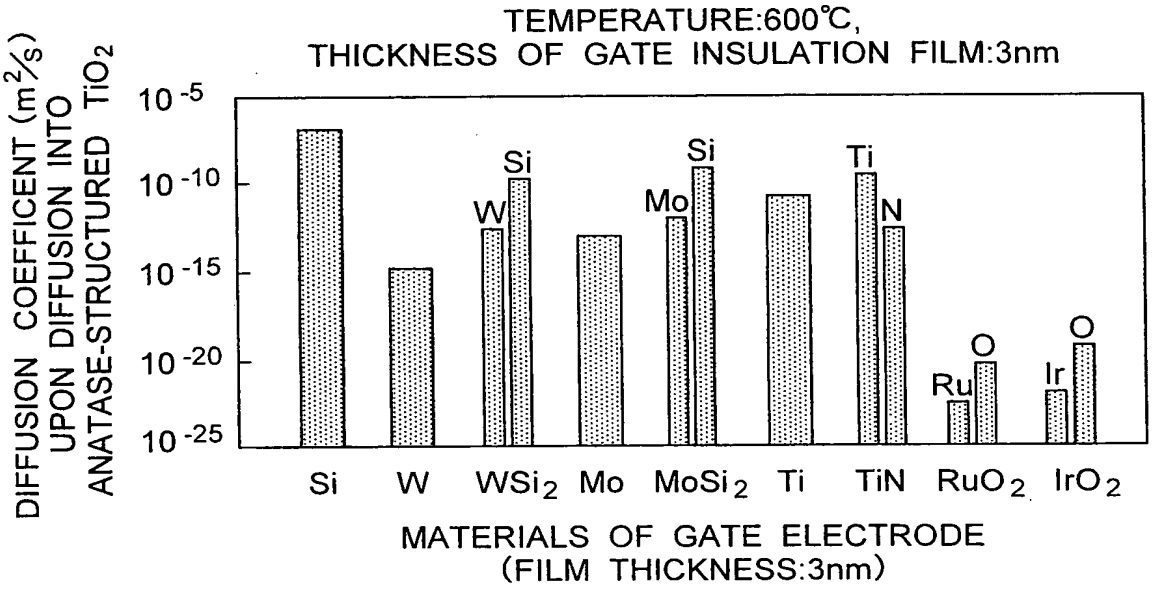
[FIG. 3]



[FIG. 4]



[FIG. 5]



[FIG. 6]

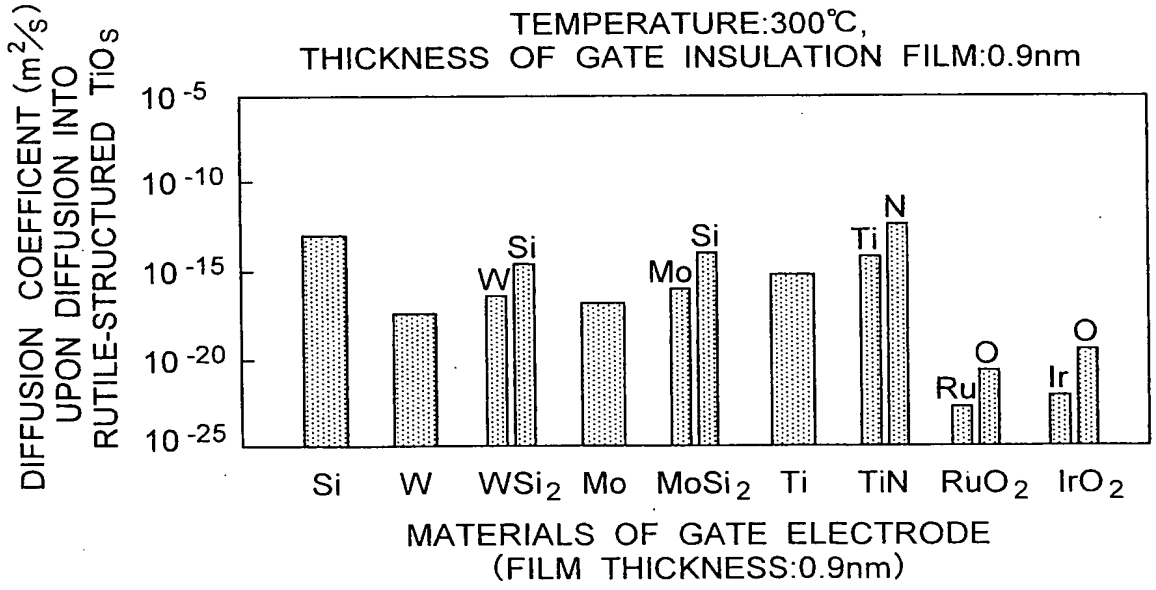


FIG. 7

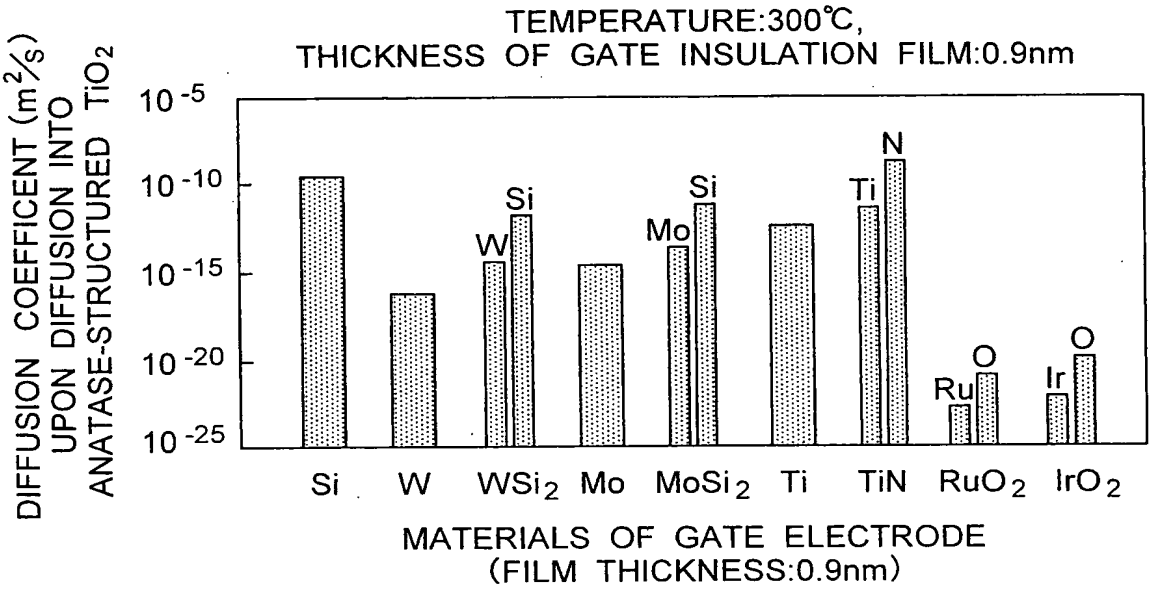


FIG. 8

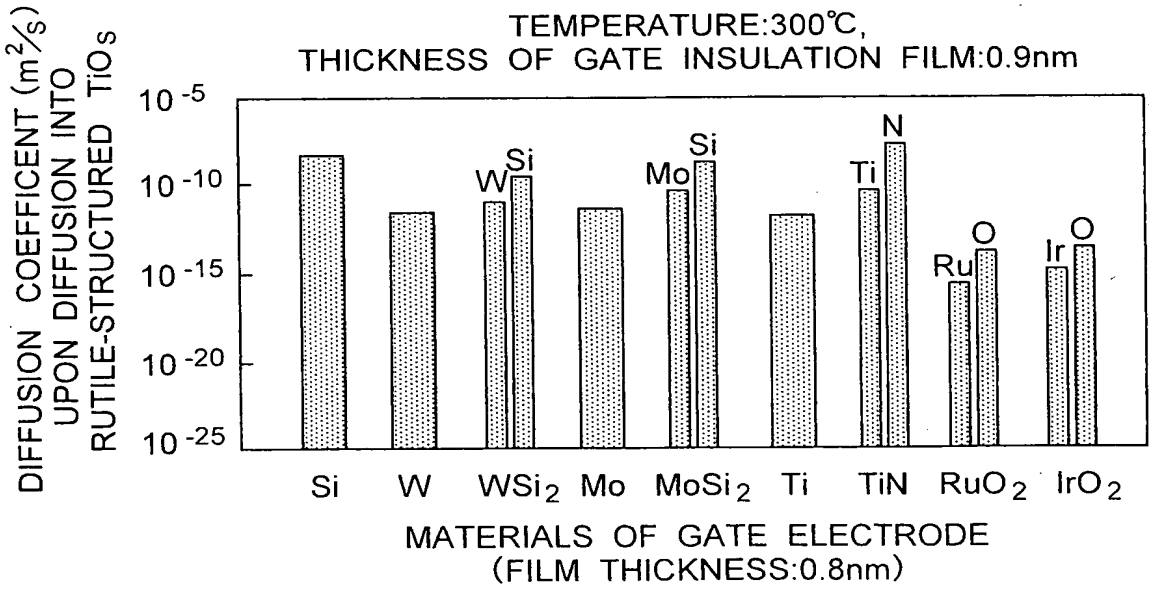


FIG. 9

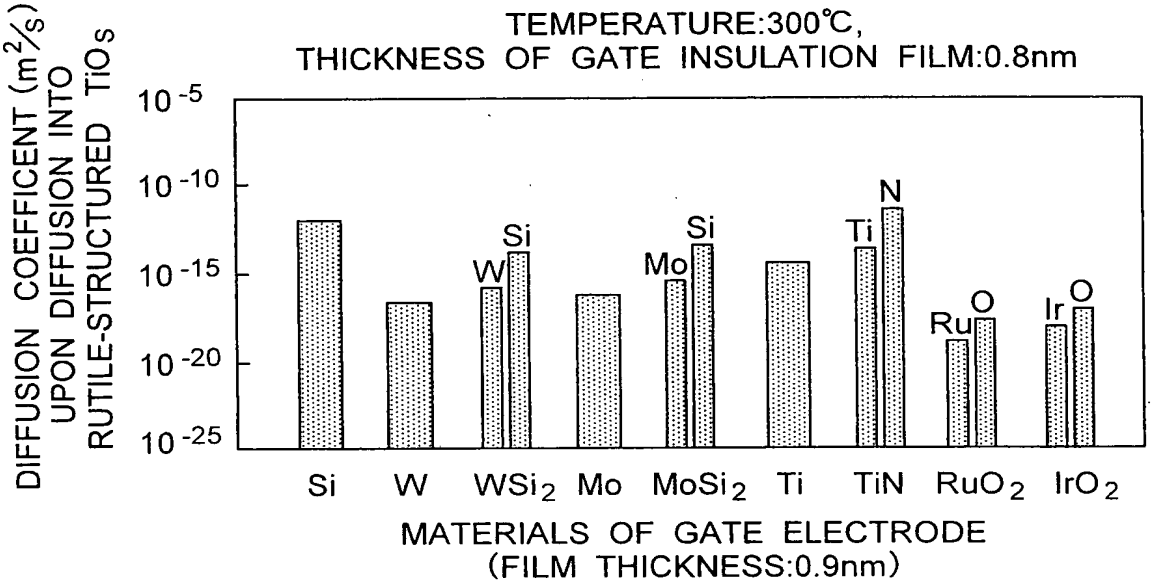

TEMPERATURE:300℃,
THICKNESS OF GATE INSULATION FILM:0.8nm
DIFFUSION COEFFICENT (m²/s)
UPON DIFFUSION INTO
RUTILE-STRUCTURED TiOs
10 -5
10 -10
10 -15
10 -20
10 -25
W
Si
Mo
Si
Ti
N
Ru
O
Ir
O
Si
W
WSi2
Mo
MoSi2
Ti
TiN
RuO2
IrO2
MATERIALS OF GATE ELECTRODE
(FILM THICKNESS:0.9nm)

FIG. 10

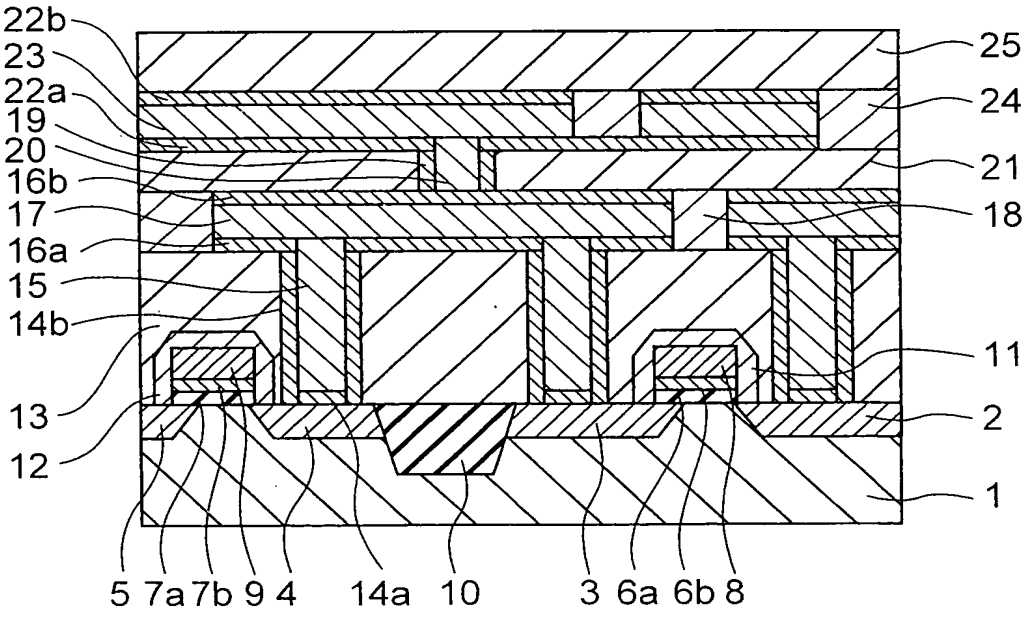

22b
23
22a
19
20
16b
17
16a
15
14b
13
12
25
24
21
18
11
2
1
5
7a
7b
9
4
14a
10
3
6a
6b
8

FIG. 11

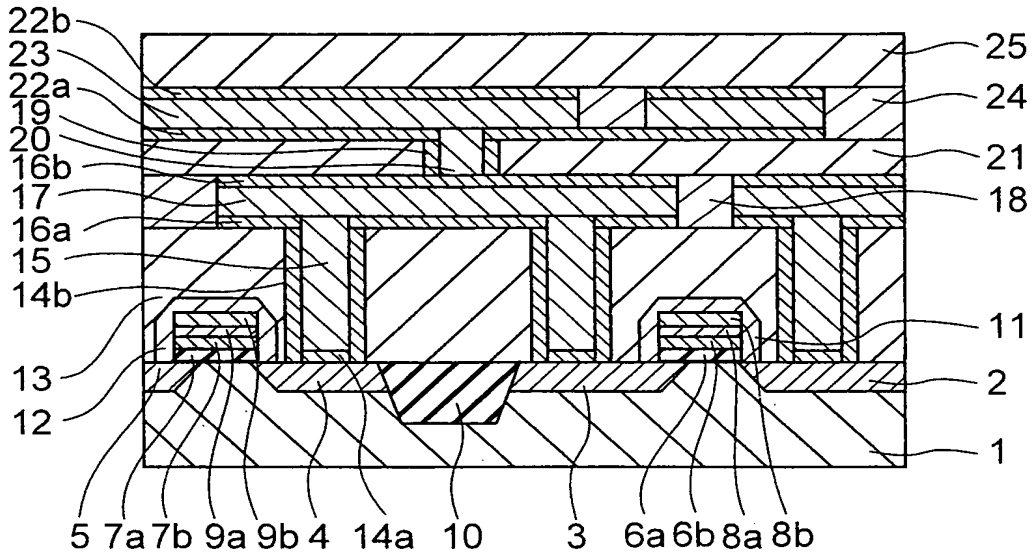
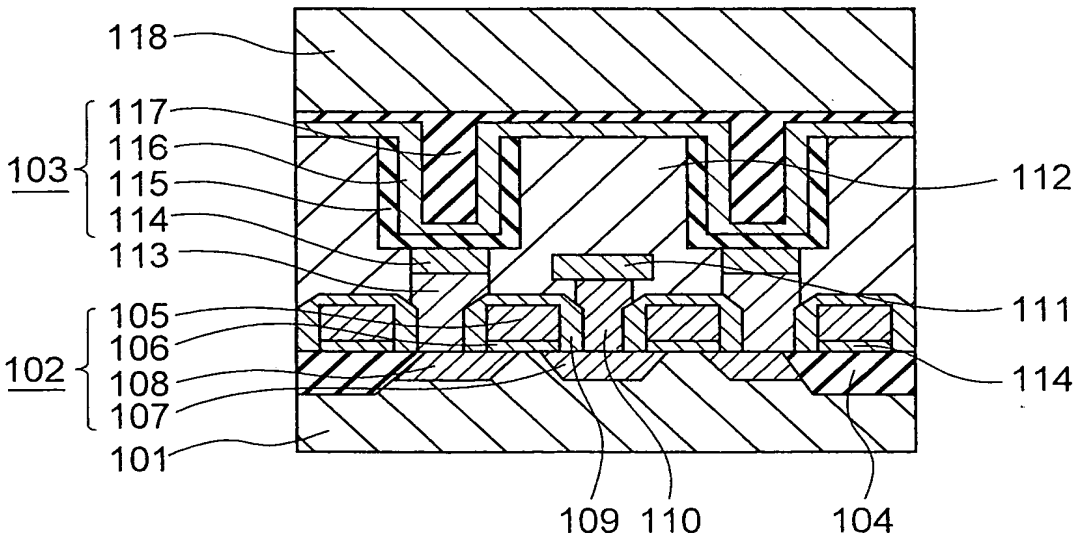


FIG. 12



[Kind of Document] Abstract

[Abstract]

[Problem] To realize a semiconductor device free of occurrence of leakage current by increasing the physical film thickness while maintaining the dielectric characteristic

[Solution] Gate insulation films 6, 7 of titanium oxide as a primary constituent material are formed on a major surface side of a silicon substrate. Gate electrode films 8, 9 are formed in contact with the gate insulation films 6, 7. Ruthenium oxide or iridium oxide is used as a primary constituent material of the gate electrode films 6, 7. The use of ruthenium oxide or iridium oxide as a primary material for the gate electrode films 8, 9, which are in contact with the titanium oxide, is effective to prevent the diffusion of conductive elements from the gate electrode films 8, 9 into the titanium oxide as the gate insulation films 6, 7. This makes it possible to realize a semiconductor device free of occurrence of leak current by increasing the physical film thickness while maintaining the dielectric characteristic.

[Selected Drawing] Fig. 1